WHAT IS CLAIMED IS:

1. A method for manufacturing non-volatile memory cells on a semiconductive substrate, comprising at least the following steps:

forming active areas in said semiconductive substrate, bounded by portions of an insulating layer;

forming a first thin layer of tunnel oxide and depositing a first layer of conductive material on said active areas;

defining a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of:

forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes;

forming spacers of a second material in the shelter of the side walls of said stripes, said second material being selectively etchable with respect to said first material,

depositing a layer of a third material in order to fill in the space between said spacers,

planarizing said layer of a third material together with said alternated stripes and said spacers,

selectively removing said spacers in order to expose portions of said first layer of semiconductive material,

etching said first layer of semiconductive material in order to form grooves in correspondence with its exposed portions,

selectively removing said alternated stripes and said layer of a third material.

2. The method according to claim 1, wherein said first material and said third material are a conductive material.

3. The method according to claim 2, wherein said plurality of alternated stripes is formed by depositing a second layer of conductive material and by defining said second layer of conductive material by means of lithography.

4. The method according to claim 3, wherein between said first layer of semiconductive material and said second layer of semiconductive material a thin oxide layer is interposed.

5. The method according to claim 1, wherein said second material is silicon nitride and wherein the formation of said spacers in the shelter of the side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of an anisotropic etching.

6. The method according to claim 1, wherein said first material and said third material are each an oxide.

7. The method according to claim 6, wherein said plurality of alternated stripes is formed by depositing a first oxide layer and by defining said first oxide layer by means of lithography.

8. The method according to claim 7, wherein said second material is silicon nitride and wherein the formation of said spacers in the shelter of the side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of an anisothropic etching.

9. A method for manufacturing non-volatile memory cells on a semiconductive substrate, comprising at least the following steps:

forming active areas in said semiconductive substrate, bounded by portions of an insulating layer;

forming a first thin tunnel oxide layer and depositing a first layer of conductive material on said active areas;

defining a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of:

forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes;

forming spacers of a second material in the shelter of the side walls of said alternated stripes, said second material being selectively etchable with respect to said first material,

selectively removing said plurality of alternated stripes,

depositing a layer of a third material between said spacers,

selectively removing said spacers in order to expose portions of said first layer of semiconductive material,

etching said first layer of semiconductive material in order to form grooves in corrispondence of its exposed portions,

selectively removing said layer of a third material.

10. The method according to claim 9, wherein said first material and said third material are respectively a conductive material and an oxide being thermally grown.

11. The method according to claim 10, wherein said plurality of alternated stripes is formed by depositing a second layer of conductive material and by defining said second layer of conductive material by means of lithography.

12. The method according to claim 11, wherein between said first layer of conductive material and said second layer of conductive material a thin oxide layer is interposed.

13. The method according to claim 9, wherein said second material is silicon nitride and wherein the formation of said spacers in the shelter of side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of an isotropic etching.

14. A method for manufacturing non-volatile memory cells on a semiconductor substrate, comprising:

forming active areas in said semiconductor substrate, bounded by portions of an insulating layer;

depositing a first thin layer of tunnel oxide and a first layer of conductive material on said active areas; and

defining a plurality of floating gate regions, comprising:

forming stripes of shielding material only above pairs of alternated active areas;

defining spacers of small width in the shelter of the side walls of the stripes thus defined;

defining stripes of shielding material also on the active areas that lacked them; and

completing the formation of the floating gates by leaving the definition of the distance between floating gate regions to the spacers.

15. A semiconductor fabrication method, comprising:

forming a plurality of first stripes over an insulated base polysilicon layer and which lie above first alternating active areas;

forming sidewall spacers for the plurality of first stripes;

forming a plurality of second stripes between the sidewall spacers over the insulated base polysilicon layer which lie above second alternating active areas; and

removing the sidewall spacers.

16. The method according to Claim 15, wherein forming the plurality of first stripes comprises:

depositing a first material layer;

defining the first stripes in the first material layer using a photolithography mask;

etching using the mask to remove the first material layer but leave the first stripes.

17. The method according to Claim 15, wherein forming the plurality of second stripes comprises:

depositing a second material layer that covers the first stripes and fills a region between sidewall spacers;

planarizing to remove the second material layer but leave the second stripes.

18. The method according to claim 15, wherein forming sidewall spacers comprises:

depositing a nitride layer; and

patterning the nitride layer to remove the nitride layer above the second alternating active areas but leave the nitride layer adjacent sidewalls of the first stripes.

19. The method according to Claim 15, further comprising:

using the first and second stripes as a hard mask; and

etching using the first and second stripes hard mask to define floating gate regions in the base polysilicon layer above both the first and second alternating active areas.

20. The method according to claim 15, wherein the first and second stripes are formed from polysilicon material.

21. The method according to claim 15, wherein the first and second stripes are formed from oxide material.

22. A method for semiconductor fabrication on a substrate including a plurality of active areas, comprising:

forming a plurality of first stripes by photolithographic techniques over an insulated base polysilicon layer and which lie above even ones of the plurality of active areas; and

forming a plurality of second stripes without the use of photolithographic techniques over the insulated base polysilicon layer and which lie above odd ones of the plurality of active areas.

23. The method of claim 22 wherein forming a plurality of first stripes comprises:

depositing a first material layer;

defining the first stripes in the first material layer using a photolithography mask;

etching using the mask to remove the first material layer but leave the first stripes.

24. The method of claim 22 wherein forming the plurality of second stripes comprises:

forming sidewall spacers for the plurality of first stripes;

forming the plurality of second stripes between the sidewall spacers over odd ones of the active areas; and

removing the sidewall spacers.

25. The method of claim 22 wherein forming the plurality of second stripes comprises:

forming sidewall spacers for the plurality of first stripes;

depositing a second material layer that covers the first stripes and fills a region between the sidewall spacers;

planarizing to remove the second material layer but leave the second .

26. The method according to claim 22, wherein forming sidewall spacers comprises:

depositing a nitride layer; and

patterning the nitride layer to remove the nitride layer above odd ones of the active areas but leave the nitride layer adjacent sidewalls of the first stripes.

27. The method according to Claim 22, further comprising:

using the first and second stripes as a hard mask; and

etching using the first and second stripes hard mask to define floating gate regions in the base polysilicon layer above both the odd and even ones of the active areas.

28. The method according to claim 22, wherein the first and second stripes are formed from polysilicon material.

29. The method according to claim 22, wherein the first and second stripes are formed from oxide material.

30. A semiconductor fabrication method, comprising:

forming a plurality of stripes over an insulated base polysilicon layer and which lie above first alternating active areas;

forming sidewall spacers for the plurality of stripes;

removing the stripes but leaving the sidewall spacers;

forming an oxide layer over the insulated base polysilicon layer between the sidewall spacers; and

removing the sidewall spacers.

31. The method according to Claim 30, wherein forming the plurality of stripes comprises:

depositing a material layer;

defining the stripes in the material layer using a photolithography mask;

etching using the mask to remove the material layer but leave the stripes.

32. The method according to claim 30, wherein forming sidewall spacers comprises:

depositing a nitride layer; and

patterning the nitride layer to remove the nitride layer above second alternating active areas but leave the nitride layer adjacent sidewalls of the stripes.

33. The method according to Claim 30, further comprising:

using the oxide layer between the removed spacers as a hard mask; and

etching using the oxide layer hard mask to define floating gate regions in the base polysilicon layer.